

Application number 09/880,734  
Amendment dated October 11, 2005  
Amendment under 37 CFR 1.116 Expedited Procedure  
Examining Group 2116

PATENT

**REMARKS/ARGUMENTS**

After entry of this amendment, claims 1-15, 44, and 46-54 will remain pending in this application. Claims 1, 4, 7, 8, 10, 44, 46, and 47 have been amended. Claims 44 and 48 were also amended to correct typographical oversights. Support for the amended claims can be found in the specification. No new matter has been added.

Claims 1-2, 4-5, and 7-14 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Van de Steeg et al., United States patent number 5,479,618 (Steeg), in view of Yokouchi et al., United States patent number 4,796,211 (Yokouchi). Claims 44, 46-51, and 53 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Yokouchi in view of Steeg.

**Claim 1**

Claim 1 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Steeg in view of Yokouchi. But these references do not show or suggest each and every element of this claim. For example, claim 1 recites "loading an initial value in a count register that is a part of a watchdog timer circuit on the programmable logic integrated circuit...and...causing reloading of configuration data from an external source into the programmable logic integrated circuit." The cited references do not provide this combination of features.

The pending office action cites Steeg as providing each of the recited features except for those relating to the operation of the watchdog timer. (See pending office action, pages 2 and 3, paragraphs 6 and 7.) But Steeg does not provide a watchdog timer and the reloading of configuration data on the same programmable logic integrated circuit as required by the claim. Rather, Steeg shows a watchdog timer on a first programmable logic circuit 29 (See Steeg, Figure 4), and the reloading of configuration data on a second programmable logic circuit 37 (See Steeg, Figure 5). For example, Steeg teaches "when a watchdog timeout is detected, a reset/clear signal is transmitted to the second programmable logic circuit. (emphasis added, see Steeg, column 8, lines 49-59.)

It is not obvious to combine these programmable logic circuits, and Steeg specifically teaches away from doing so. As stated in the background section of Steeg, two

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programmable logic circuits are used to “electrically isolate 120-volt AC signals or 24-volt DC signals, for example, on the machine side of the controller, from the 5-volt logic-level signals within the controller electronics.” (See Steeg, column 1, lines 32-38.)

This electrical isolation is achieved in Steeg through the use of optical coupling circuits 32, 33, and 34 that “provide physical and electrical isolation between the controller electronics and the controlled machine or process.” (See Steeg, column 4, lines 12-15.) The optical coupling circuits 32, 33, and 34 are between the first programmable circuit 29 and the second programmable circuit 37. (See Steeg, Figure 2.)

Thus, the first programmable logic circuit 29, which includes the watchdog timer, is isolated from the second programmable logic circuit 37, which is the circuit that is reconfigured. Not only are they isolated, but they are physically and electrically isolated. Thus, not only does Steeg teach away from combining these, but teaches that they should be physically separate circuits.

For at least this reason, claim 1 should be allowed.

Other claims

Claim 44 should be allowed for similar reasons as claim 1. The other claims depend on these claims, and should be allowed for similar reasons, and for the additional limitations they recite.

CONCLUSION

In view of the foregoing, Applicants believe all claims now pending in this application are in condition for allowance and an action to that end is respectfully requested.

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If the Examiner believes a telephone conference would expedite prosecution of this application, please telephone the undersigned at 415-576-0200.

Respectfully submitted,



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